TPCT's

College of Engineering, Osmanabad

Laboratory Manual

Digital Logic Design

For

Second Year Students

Manual Prepared by

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TPCT's

College of Engineering

Solapur Road, Osmanabad

Department of Electronics &Telecommunication

Vision of the Department:

To be recognized by the society at large as an excellent department offering quality higher education in the Electronics & Telecommunication Engineering field with research focus catering to the needs of the public and being in tune with the advancing technological revolution.

Mission of the Department:

To achieve the vision the department will

- Establish a unique learning environment to enable the student's face the challenges of the Electronics & Telecommunication Engineering field.
- Promote the establishment of centers of excellence in technology areas to nurture the spirit of innovation and creativity among the faculty & students.
- Provide ethical & value based education by promoting activities addressing the needs of the society.
- Enable the students to develop skill to solve complete technological problems of current times and also to provide a framework for promoting collaborative and multidisciplinary activities.

College of Engineering

Technical Document

This technical document is a series of Laboratory manuals of Electronics and Telecommunication Department and is a certified document of College of engineering, Osmanabad. The care has been taken to make the document error-free. But still if any error is found, kindly bring it to the notice of subject teacher and HOD.

Recommended by,

HOD

Approved by,

Principal

FOREWORD

It is my great pleasure to present this laboratory manual for second year engineering students for the subject of **Digital Logic Design** to understand and visualize the basic concepts of various circuits using electronic components. Digital Logic Design covers basic concepts of electronics. This being a core subject, it becomes very essential to have clear theoretical and designing aspects.

This lab manual provides a platform to the students for understanding the basic concepts of Digital Logic Design. This practical background will help students to gain confidence in qualitative and quantitative approach to electronic circuits.

H.O.D
ECT Dept

LABORATORY MANUAL CONTENTS

This manual is intended for the Second Year students of ECT branches in the subject of Digital Logic Design. This manual typically contains practical/ Lab Sessions related to Digital Logic Design covering various aspects related to the subject for enhanced understanding.

Students are advised to thoroughly go through this manual rather than only topics mentioned in the syllabus as practical aspects are the key to understanding and conceptual visualization of theoretical aspects covered in the books.

SUBJECT INDEX:

Dos and Don'ts in Laboratory :-

1. Do not handle any equipment before reading the instructions /Instruction manuals.
2. Read carefully the power ratings of the equipment before it is switched ON, whether ratings 230 V/50 Hz or 115V/60 Hz. For Indian equipment, the power ratings are normally 230V/50Hz. If you have equipment with 115/60 Hz ratings, do not insert power plug, as our normal supply is 230V/50Hz., which will damage the equipment.
3. Observe type of sockets of equipment power to avoid mechanical damage.
4. Do not forcefully place connectors to avoid the damage.
5. Strictly observe the instructions given by the Teacher/ Lab Instructor.

Instruction for Laboratory Teachers:-

1. Submission related to whatever lab work has been completed should be done during the next lab session.
2. Students should be instructed to switch on the power supply after getting the checked by the lab assistant / teacher. After the experiment is over, the students must hand over the Bread board, wires, CRO probe to the lab assistant/teacher.
3. The promptness of submission should be encouraged by way of marking and evaluation patterns that will benefit the sincere students.

2. Lab Exercises

PART A:

Experimentation using digital ICs.

1. Operation of Arithmetic building blocks;
2. Study of Arithmetic logic unit (ALU IC 74181);
3. Code conversion operations: Binary to Gray
4. Code conversion operations: Gray to Binary;
5. Multiplexers;
6. Demultiplexers, Decoders & Encoders;
7. Study of flip-flops: RS, JK, MSJK, D & T;
8. Counter Design Using ICs;
9. Shift registers Using ICs;

PART B:

10.Experimentation using VHDL Code

Write, simulate and verify, VHDL Code for;

1. Logic gates.;
2. Half adder/full adder.;
3. Gray to binary/binary to gray;
4. D Flip-flop.;

Pre-Lab

Introduction to different digital gate ICs;

Basic Gate:

- AND Gate: The **AND gate** performs a logical "and" operation on two inputs, A and B:

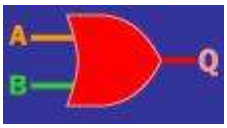
AND Gate

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

- OR Gate: The **OR gate** performs a logical "or" operation on two inputs, A and B:

OR Gate

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1



- NOT Gate: The simplest possible gate is called an "inverter," or a **NOT gate**. It takes one bit as input and produces output as its opposite. The logic table for NOT gate and its symbol are shown below.

NOT Gate

A	Q
0	1
1	0

Universal Gate

- NAND Gate: It is quite common to recognize two others as well: the **NAND** and the **NOR** gate. These two gates are simply combinations of an AND or an OR gate with a NOT gate.

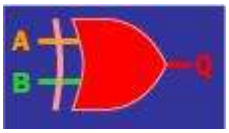
NAND Gate

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

- EX-OR Gate: The final two gates that are sometimes added to the list are the **XOR** and **XNOR** gates, also known as "exclusive or" and "exclusive nor" gates, respectively. Here are their tables:

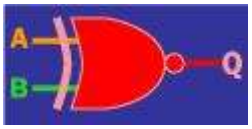
XOR Gate

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0



XNOR Gate

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1



EXPERIMENT NO. 1

Operation of Arithmetic building blocks;

Aim: To design and Realize circuit of Half adder and full adder.

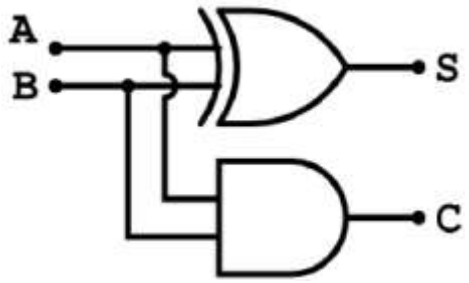
Objectives:

1) To construct half adder circuit and verify its working.

2) To construct full adder circuit and verify its working.

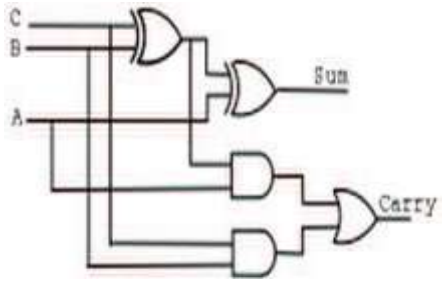
Apparatus: Bread board , wires IC-7486(EX-OR),7408(AND)

Circuit diagram :



Circuit diagram of Half Adder

INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Circuit diagram of Full Adder

INPUT			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1

Theory:-

A logic circuit for the addition of two one bit numbers is referred to as an half adder. A half adder can be constructed using EX-OR(IC-7486) and AND (IC7408) gates. The truth table shows, that in the first three rows there is no carry, whereas in the fourth row a carry is present. From the truth table, we obtain the logical expression for SUM and CARRY as,

SUM=A'B+AB'
CARRY=AB

Half Adder/Subtractor is a basic ckt. that adds / subtracts 2 bits and generates sum or difference along with Carry / Borrow. Unlike half adder or subtractor a full adder / subtractor has the provision to take consideration of previous carry / borrow also.

Procedure:-

1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7
2) Assemble the circuit on bread board.
3) Give the logical inputs and check for the proper output.

Conclusion: Hence verified Half Adder operation.

Experiment No.2

Arithmetic Logic Unit(ALU)

Aim: To study various logic and Arithmetic operations using IC 74181 ALU

Apparatus: Bread board , wires , IC 74181

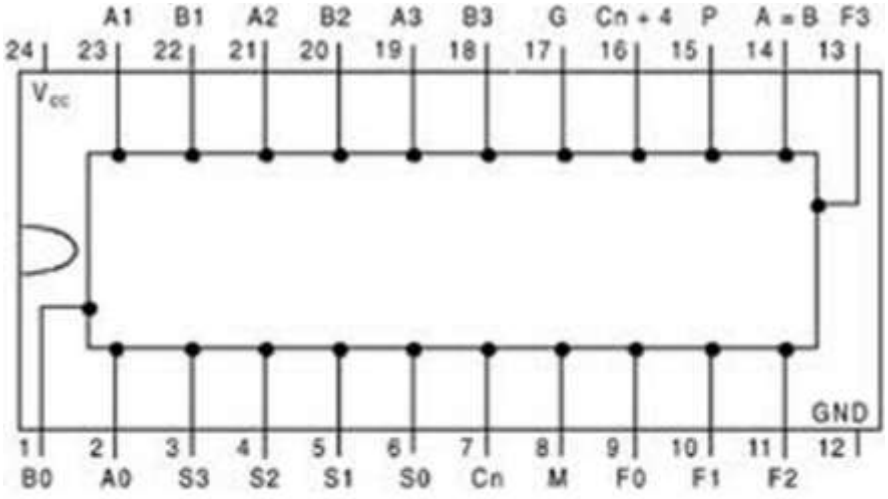
Objective: i)To study operation of arithmetic logic .

ii)To implement ckt. of ALU using 74181 IC and realize both the operations.

Theory :

The TTL-series 4-bit 74181 arithmetic-logical unit takes 4-bit operands and a carry input and calculates one of 16 logical or 16 arithmetic functions. Two additional active-low outputs X (/propagate) and Y (/generate) allow to interface to the 74182 carry-look ahead generator IC for fast addition.

The M input selects whether the ALU should calculate logical functions (M=1) or arithmetic functions (M=0). In each mode, the four S3..S0 inputs select one of the available operations; check the table in the schematics for the specific functions selected by each select input. For example, M=0 and S=(1001) select the normal binary addition including carry, Z=(A+B+Cin).



Pin diagram of IC 74181

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS $(A + \overline{B})$	F = A PLUS $(A + \overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS $(A + \overline{B})$	F = AB PLUS $(A + \overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	F = $(A + \overline{B})$ PLUS 1
H	L	L	L	$F = \overline{AB}$	F = A PLUS (A • B)	F = A PLUS (A • B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A • B)	$F = A\overline{B}$ PLUS (A • B) PLUS 1
H	L	H	H	F = A • B	F = (A • B)	F = (A • B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A[‡]	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

[‡]Each bit is shifted to the next more significant position.

Procedure:

Assemble the circuit on bread board and verify various logic and Arithmetic operations according to select inputs.

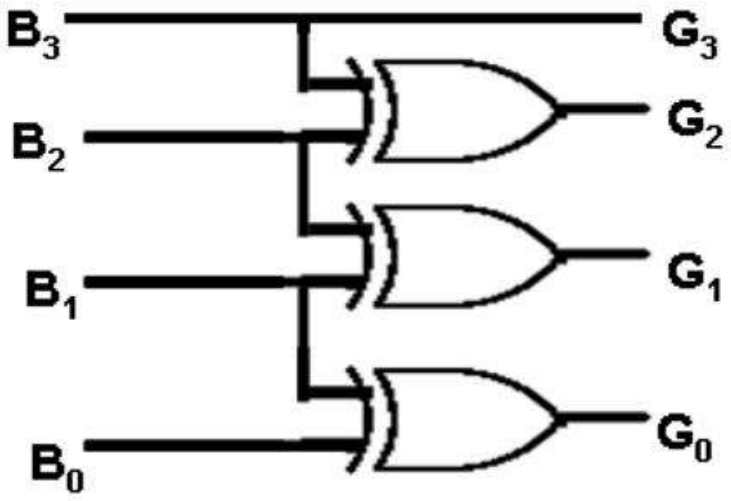
Conclusion: Hence ,studied the various logic and Arithmetic operations using IC 74181 ALU

Experiment No.3
Binary to Gray Code Conversion

Aim: To perform Binary to Gray Code Conversion

Apparatus : Bread board , wires IC-7486(EX-OR)
Objectve: i) To minimize the K-map for binary to gray code conversion and realize the logical equation using gate.
Circuit Diagram:

Figure below shows circuit diagram of binary to gray code conversion & its truth table



Circuit Diagram of Binary to Gray code Conversion

Theory :

Digital codes are required to handle data which may be numeric, Alphabets or special characters. Since digital circuits work in binary manner, therefore numerals and other characters are to be converted to binary format. This conversion process is known as encoding.

Gray code:

This code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers. For example,0111 represents 5 and 0101 represents 6 in Gray code .These two consecutive numbers differ only in one bit (third from left).Its primary application is in the location of angles on a rotating shaft.

Truth Table:

BINARY NUMBERS				CONVERTED GARY CODE NUMBERS			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Procedure:

1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7 .
2) Assemble the circuit on bread board, as per above diagram.
3) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified Binary to Gray code conversion operation.

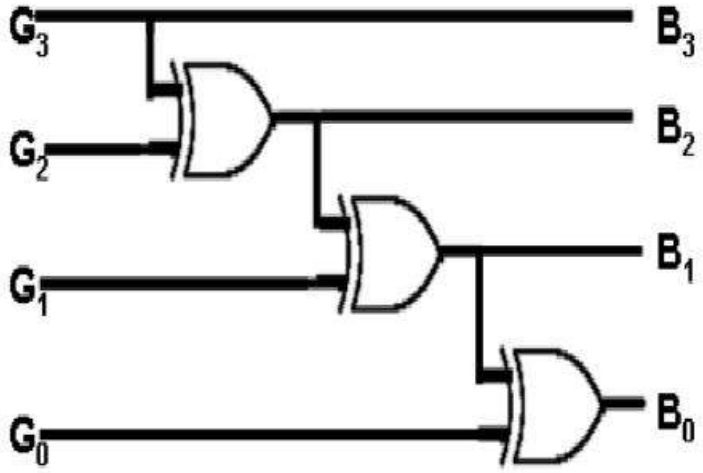
Experiment No.4

Gray code to Binary code conversion

Aim: To perform gray code to binary code conversion.

Apparatus: Bread board, wires IC-7486(EX-OR)
Objective: To minimize the K-map for gray to binary code conversion and realize the logical equation using gate.
Circuit Diagram:

Figure below shows circuit diagram of gray code to binary conversion & its truth table.



Circuit Diagram for Gray to Binary Conversion

Theory :

Digital codes are required to handle data which may be numeric, alphabets or special characters. Since digital circuits work in binary manner, therefore numerals and other characters are to be converted to binary format. This conversion process is known as encoding.

Gray code:

This code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between

successive numbers. For example,0111 represents 5 and 0101 represents 6 in Gray code .These two consecutive numbers differ only in one bit (third from left).Its primary application is in the location of angles on a rotating shaft.

Truth Table:

GARY CODE NUMBERS				CONVERTED BINARY NUMBERS			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Procedure:

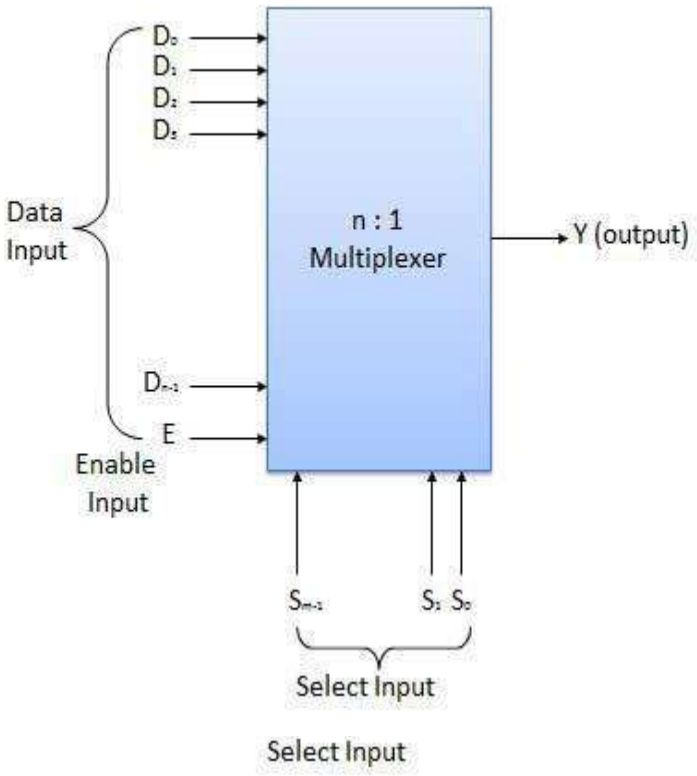
1) Apply Vcc to pin number 14 of both IC's & ground to pin number 7
2) Assemble the circuit on bread board, as per above diagram.
3) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified Gray code to Binary conversion operation

Experiment No.5

Aim: To study Multiplexer operation using IC-74153

Apparatus: Bread board , wires .
Objective: To verify the Multiplexer operation using IC-74153(4:1) MUX
Circuit Diagram: Figure below shows the block diagram of a Multiplexer.



Block diagram of a Multiplexer

Theory :

A Multiplexer (or a data selector) is a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output. The selection of the desired data input is controlled by the select (or address) inputs. In this diagram the inputs and outputs are indicated by means of arrows . Depending upon the digital code applied at the SELECT inputs, one out of the data sources is selected and

transmitted to the single output channel. The Multiplexer becomes enabled when the strobe signal is active LOW.

Note :- There are various Multiplexers available ex:74151 (8:1),74152---etc. one can refer to data sheet for specification and pin Configuration

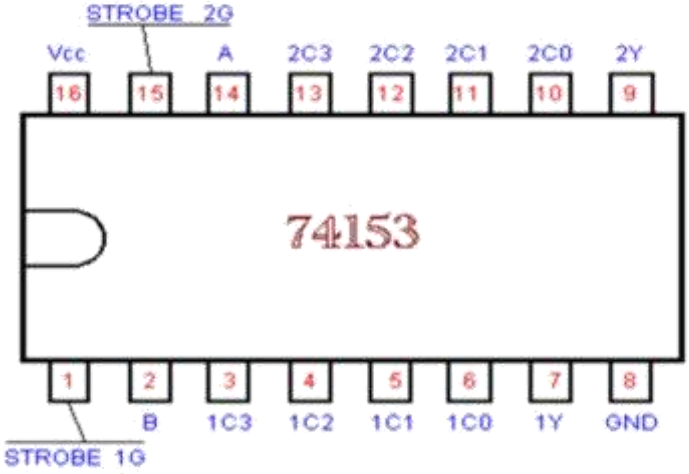


Fig 1 Pin diagram of IC 74153

Table 1 function table of IC 74153

Inputs							o/p
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Procedure:

1) Assemble the circuit on bread board, as per above diagram.
2) Give the logical inputs and check for the proper output, as per the truth table.

Conclusion: Hence verified the Multiplexer(4:1) operation using IC-74153

Experiment No.6
Demultiplexer/Decoder

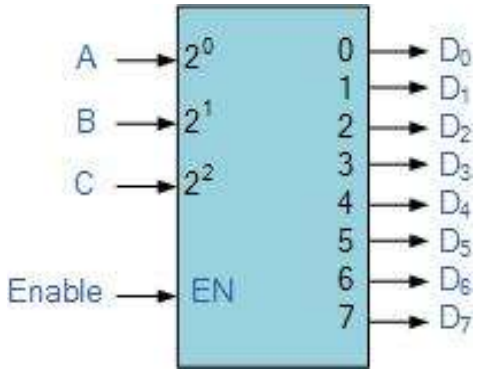
Aim: To study Demultiplexers/Decoder operation using IC-74138

Apparatus: Digital trainer kit, gate IC, wires .

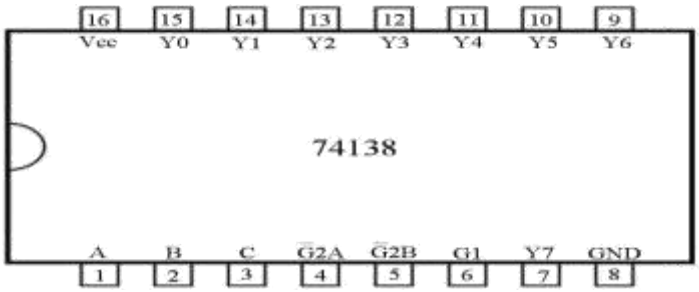
Objective: 1)To verify Demultiplexers/Decoder operation
2)One input and many output using 74138IC

Circuit Diagram:

Figure below shows the block diagram of a Decoder.



74LS138 Decoder



Pin diagram of a decoder 74LS138

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = \overline{G2A} + \overline{G2B}$
H = high level, L = low level, X = irrelevant

Depending upon the digital code applied at the SELECT inputs, one data is transmitted to the single output channel out of many. There are various Demultiplexers/Decoder available ex: 74156 1of 4 Decoder,74139---etc one can refer to data Sheet for specification and pin Configuration

Procedure:

1) Assemble the circuit on bread board, as per above Pin diagram.
2) Give the logical inputs and check for the proper output, as per the function table.

Conclusion: Hence verified the decoder (8::1) operation using IC-74138

Experiment No.7
Flip-Flop

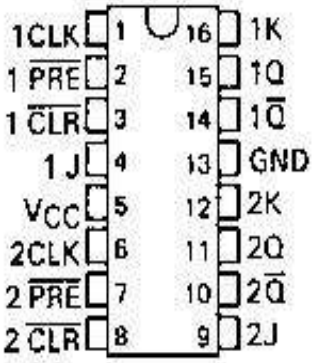
Aim: To verify truth table for JK .D and T flip-flop.

Apparatus: Bread board , wires .IC 7476(JK flip-flop),IC7474(D flip-flop)

Objective: To design various types of Flip-Flops and verify the Truth table.

Circuit Diagram:

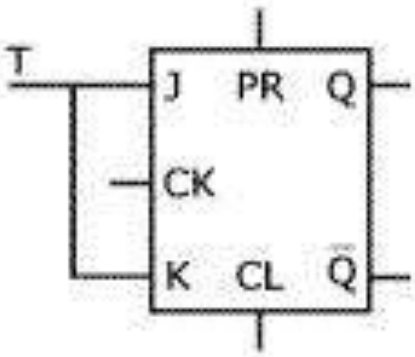
SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓	L	L	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

pin diagram and Function table of 7476



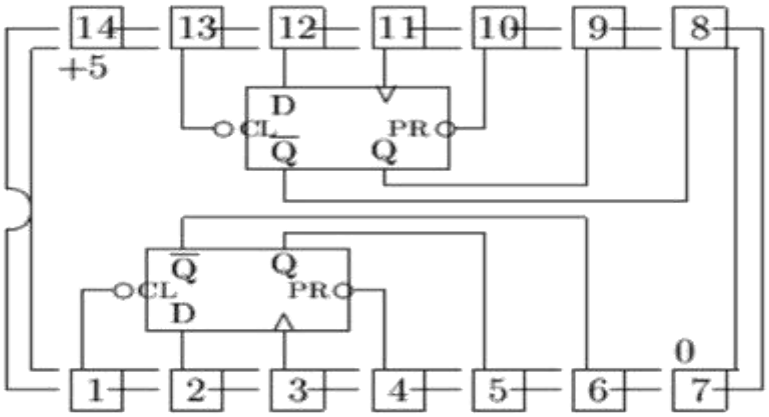
JK Flip Flop as T Flip flop

Theory:

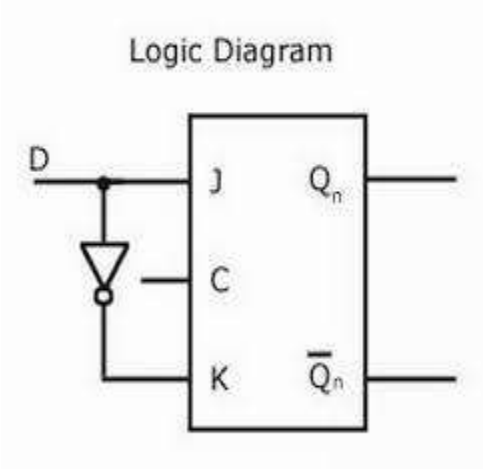
1 Explain operation of SR flip flop, master slave JK flip flop with diagram.
2 Explain race around condition.
3 Draw symbols of JK,SR,D,T Flip Flops with truth tables.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H↑	H↑
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$



Function table and pin diagram of IC 7474 D flip flop



JK Flip-Flop as D flip flop

Procedure:

1) Assemble the circuit on bread board, as per Pin diagram.
2) Verify operation of flip flops according to function /truth table

Conclusion: Hence verified flip flop operation using IC 7476 and IC 7474.

Experiment No.8

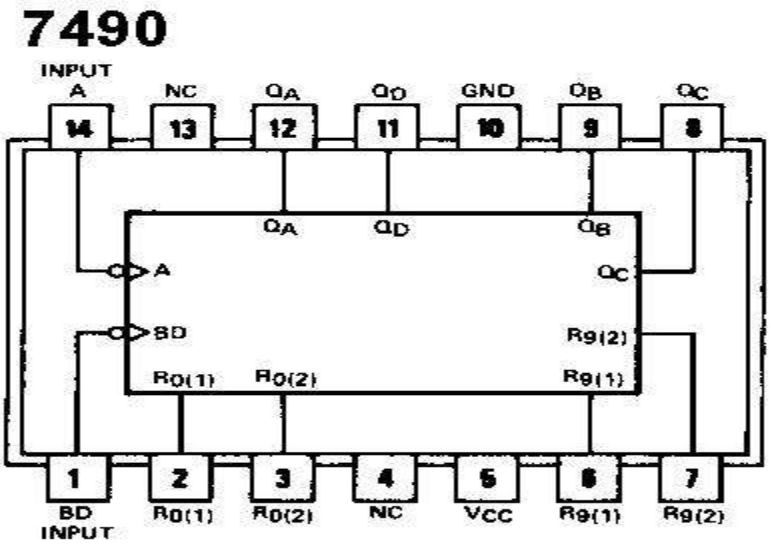
Aim: To study Decade Counter using IC-7490

Apparatus: Bread board , wires .

Objective: To design counter using IC 7490 as a decade counter.

Circuit Diagram:

Figure below shows the internal structure of 7490.



Theory :

A circuit used for counting the pulses is known as a Counter. Basically there are two types of counter:

1. Asynchronous counter (ripple counter)
2. Synchronous counter

In case of asynchronous counter all the flip-flops are not clocked simultaneously, whereas in a Synchronous counter all the flip-flops are clocked simultaneously. A Ring counter and twisted ring counter is the examples of synchronous counter.

It consists of four flip-flop internally connected to provide a mod-2 and a mod-5 counter. The mod -2 and mod-5counters can be used independently or in combination. There are two reset inputs R0(1)and R0(2) both of which are to be connected to logic 1 level for clearing all the flip-flops. The two inputs R9(1) and R9(2) when connected to logic 1 level, are used for setting the counter to 1001.

Count	QD (11)	QC (8)	QB (9)	QA (12)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Procedure:

1) Assemble the circuit on bread board, short Pin no.12 and 1
2) Give the Clock/trigger signal manually or auto clock at pin no.14 and check the count sequence.

Conclusion: Hence ,studied the decade counter using IC-7490

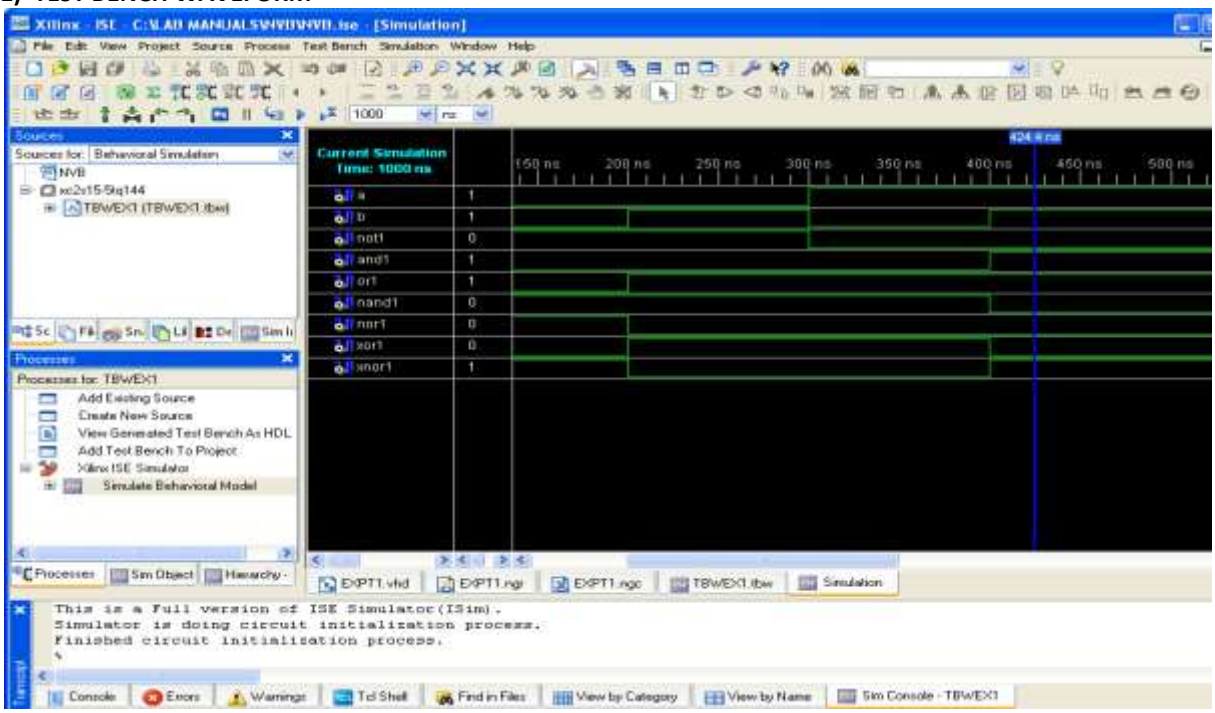
PART-B
EXPERIMENT NO 10(a)

Project Name: **DESIGN OF LOGIC GATES**
-- Target Devices: **SPARTAN2**
-- Tool versions: **ISE10.1**

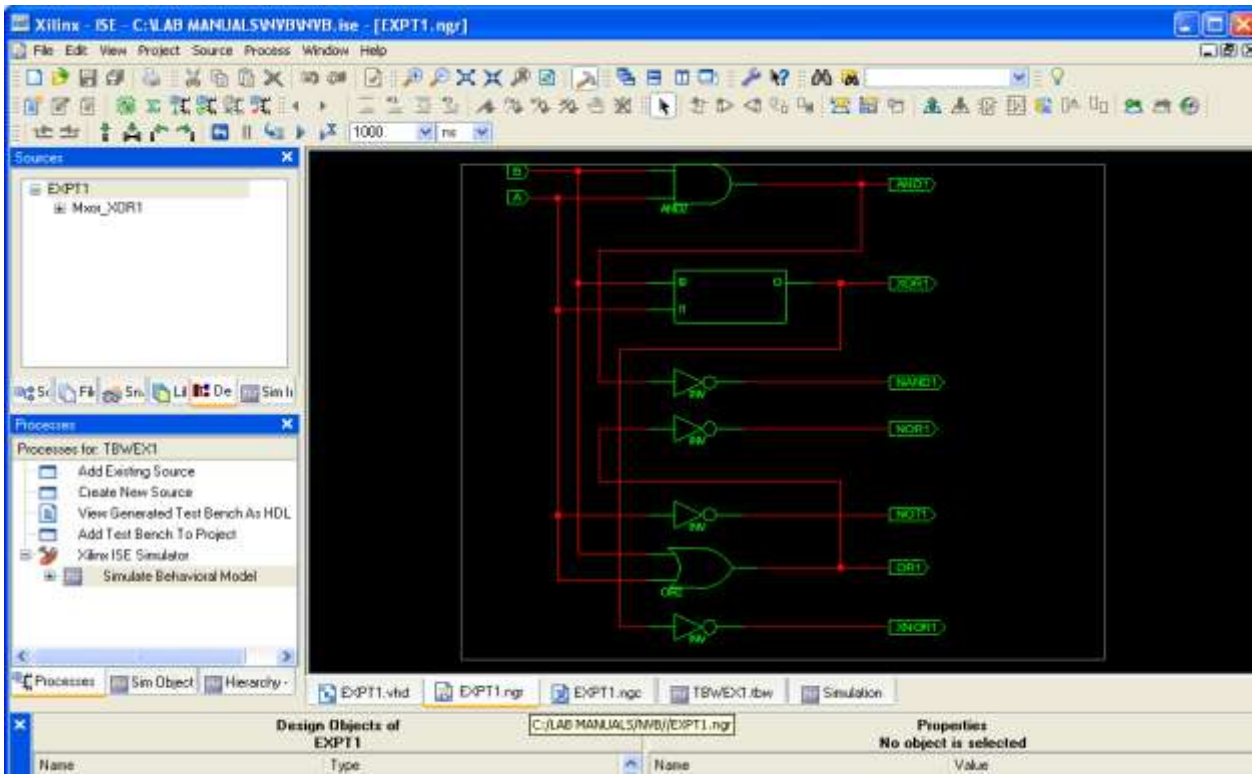
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity EXPT1 is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          NOT1 : out  STD_LOGIC;
          AND1 : out  STD_LOGIC;
          OR1 : out  STD_LOGIC;
          NAND1 : out  STD_LOGIC;
          NOR1 : out  STD_LOGIC;
          XOR1 : out  STD_LOGIC;
          XNOR1 : out  STD_LOGIC);
end EXPT1;
architecture Behavioral of EXPT1 is
begin
NOT1 <= NOT A;


AND1 <= A AND B;
OR1 <= A OR B;
NAND1 <= A NAND B;
NOR1 <= A NOR B;
XOR1 <= A XOR B;
XNOR1 <= A XNOR B;
end Behavioral;
```

SIMULATION RESULT:

1) TEST BENCH WAVEFORM



2) RTL SCHEMATIC

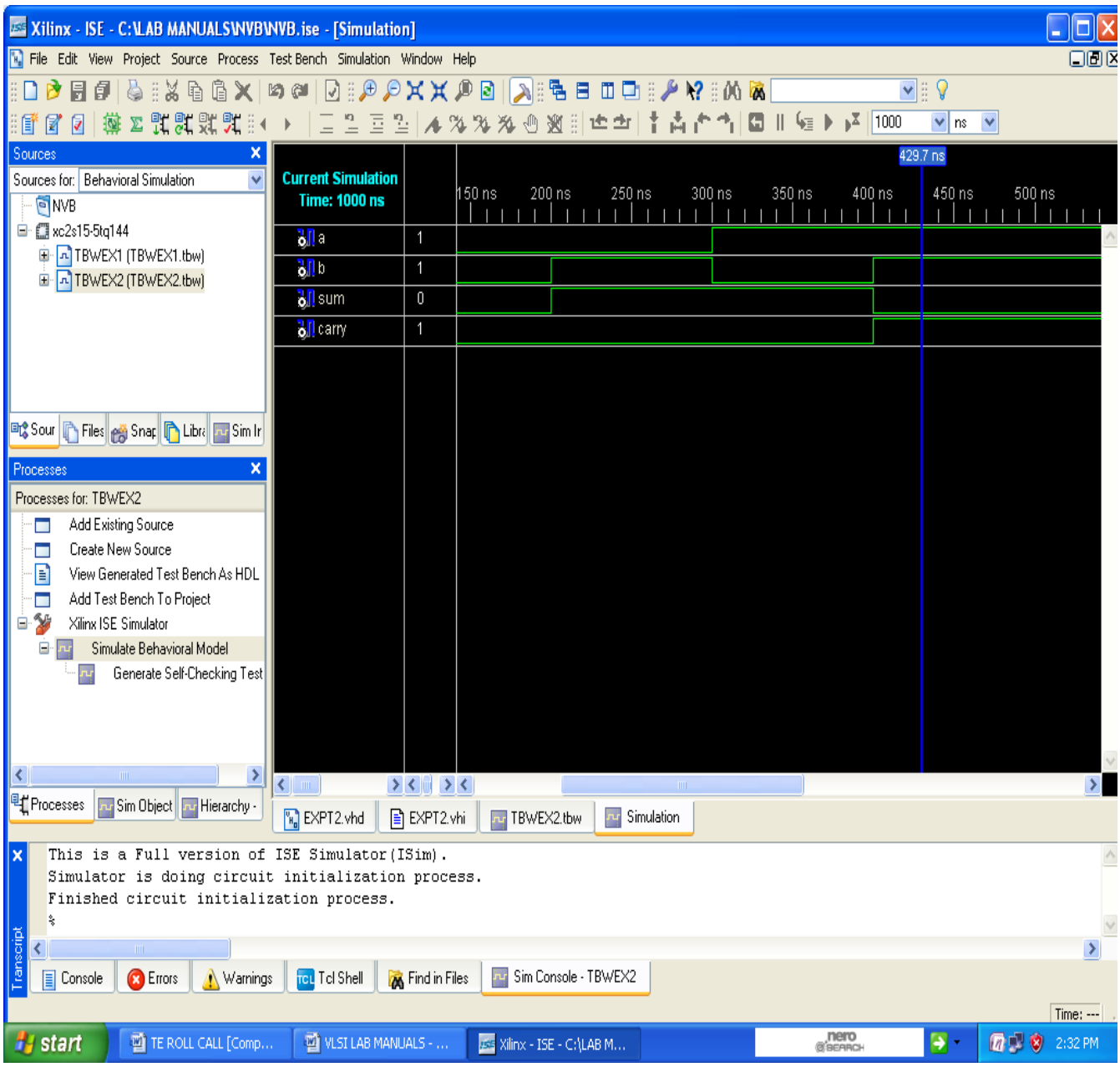


EXPERIMENT NO 10(b)

-- Project Name: **HALF ADDER USING DATAFLOW STYLE**
-- Target Devices: **SPARTAN2**
-- Tool versions: **ISE 10.1**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity EXPT2 is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          CARRY : out  STD_LOGIC);
end EXPT2;
architecture Behavioral of EXPT2 is
begin
SUM <= A XOR B;
CARRY <= A AND B;
end Behavioral;
```

SIMULATION RESULT:

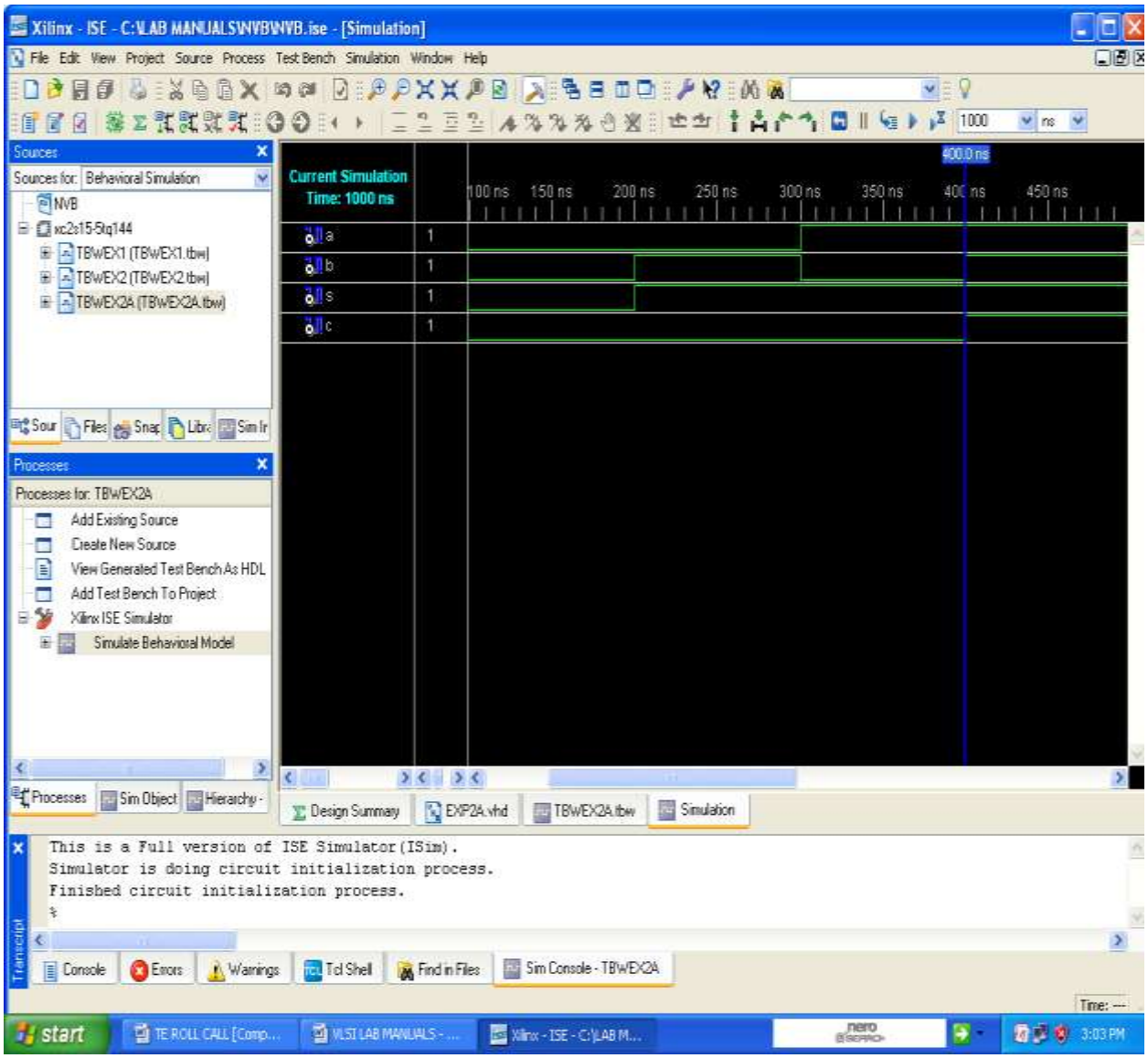


EXPERIMENT NO.10(c)

```
----------------------------------------------------------------------------------
-- Project Name: HALF ADDER USING BEHAVIORAL STYLE
-- Target Devices: SPARTAN 2
-- Tool versions: ISE 10.1
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity EXP2A is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           S : out  STD_LOGIC;
           C : out  STD_LOGIC);
end EXP2A;
architecture Behavioral of EXP2A is
begin
process (A,B)
begin
if (A= '0')then
 if (B = '0')then
 s <= '0';
 c <= '0';
else
 s <= '1';
 c <= '0';
 end if;
 else
 if (B = '0')then
 s <= '1';
 c <= '0';
 else
  s <= '1';
  c <= '1';
  end if;
  end if;
  end process;
```

end Behavioral;

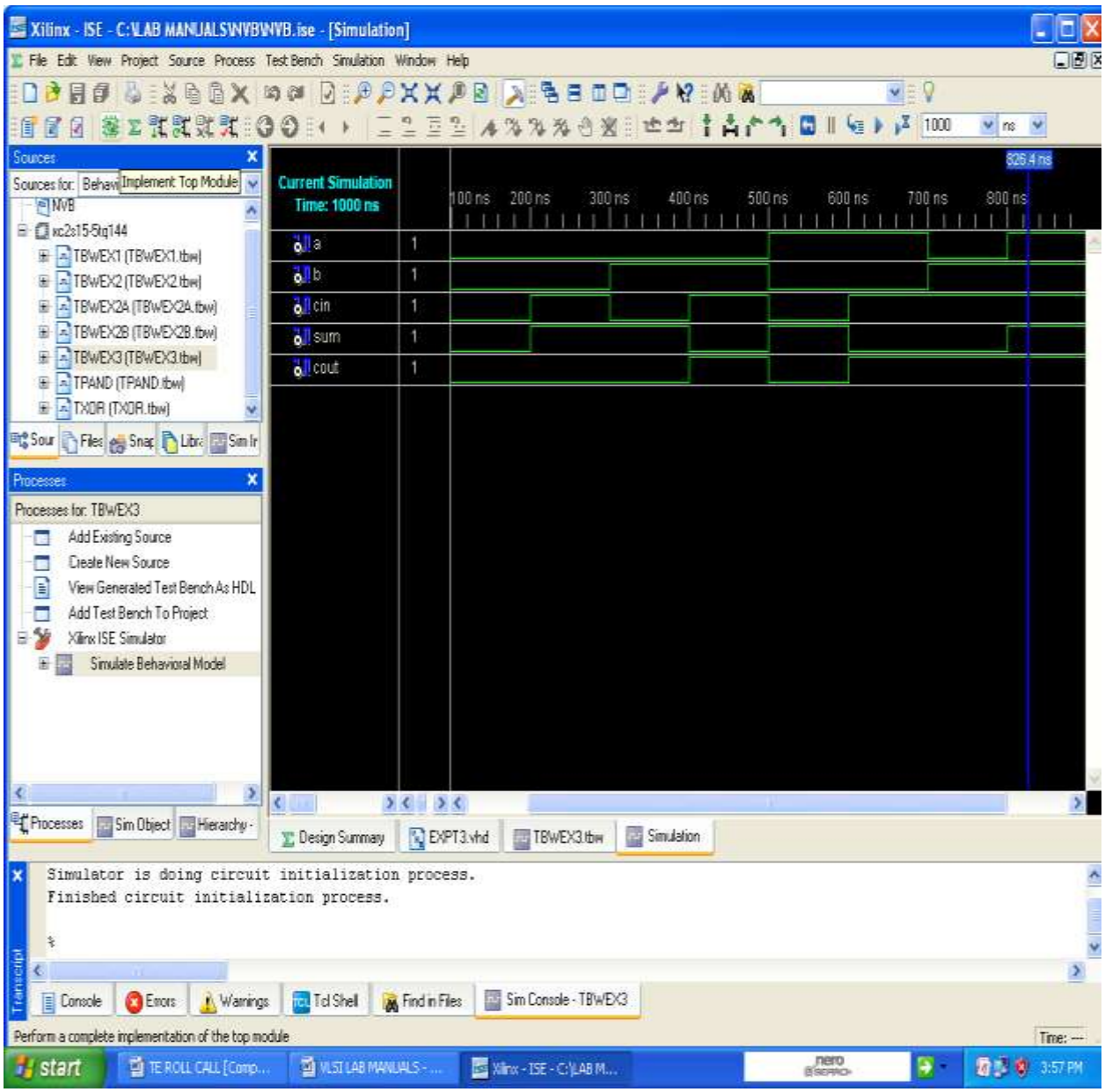
SIMULATION RESULT:



EXPERIMENT NO .10(c)

```
----------------------------------------------------------------------------------
-- Project Name: DESIGN OF FULL ADDER
-- Target Devices: SPARTAN 2
-- Tool versions: ISE 10.1
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity EXPT3 is
   Port ( A : in  STD_LOGIC;
          B : in  STD_LOGIC;
          Cin : in  STD_LOGIC;
          SUM : out  STD_LOGIC;
          Cout : out  STD_LOGIC);
end EXPT3;
architecture Behavioral of EXPT3 is
signal X: STD_LOGIC;
begin
X <= (A XOR B)AND Cin;
SUM <= A XOR B XOR Cin;
Cout <= X OR (A AND B);
end Behavioral;
```

SIMULATION RESULT:



3.Quiz on the subject:-

A) Viva-voce questions:

1. What do you mean by Logic Gates?
2. What are the applications of Logic Gates?
3. What is Truth Table?
4. Why we use basic logic gates?
5. Write down the truth table of all logic gates?
6. What do you mean by universal gate?
7. Write truth table for 2 I/P OR, NOR, AND and NAND gate?
8. Implement all logic gate by using Universal gate?
9. Why is they called Universal Gates?
10. Give the name of universal gate?
11. Draw circuit diagram of Half Adder circuit?
12. Draw circuit diagram of Full Adder circuit?
13. Draw Full Adder circuit by using Half Adder circuit and minimum no. of logic gate?
14. Write Boolean function for half adder? Q.5 Write Boolean function for Full adder?
15. Design the half Adder & Full Adder using NAND-NAND Logic.
16. Draw circuit diagram of Half Subtractor circuit?
17. Draw circuit diagram of Full Subtractor circuit?
18. Draw Full Subtractor circuit by using Half Subtractor circuit and minimum no. of logic gate?
19. Write Boolean function for half Subtractor?
20. Write Boolean function for Full Subtractor?
21. What is Excess-3 code? Why it is called Excess-3 code?
22. What is the application of Excess-3 Code?
23. What is ASCII code?
24. Excess-3 code is Weighted or Unweighted?
25. Out of the possible 16 code combination? How many numbers used in Excess-3 code?
26. What is Demorgan's Law?
27. Show the truth table for Demorgan's Theorem?
28. What is Minterm & Maxterm?
29. How Minterm can be converted in Max term?
30. What is Hybrid function?
31. What is Flip-Flop?
32. What is Latch circuit?
33. Draw a truth –tables of S-R, J-K, D and T?

34. What is the disadvantages of S-R Flip-Flop?
35. How can you remove the problem of S-R Flip –Flop?
36. Make circuit diagram of S-R, J-K, D and T Flip-Flop?
37. What do you understand by Race Aground condition? How it is over come in J-K Flip Flop?
38. Explain the principle of Multiplexer?
39. Draw a circuit diagram of 4: 1 Multiplexer?
40. What are the advantages of Multiplexer?
41. What are the disadvantages of Multiplexer?
42. Make the Truth-table of Multiplexer?
43. Explain about Demultiplexers?
44. Draw a circuit diagram of 1: 4 Demultiplexers?
45. Make a logic diagram of 1: 4 Demultiplexers?
46. What is the application of Demultiplexers?
47. What is the difference between Multiplexer and Demultiplexers?

4. Conduction of Viva-Voce Examinations:

Teacher should conduct oral exams of the students with full preparation. Normally, the objective questions with guess are to be avoided. To make it meaningful, the questions should be such that depth of the students in the subject is tested. Oral examinations are to be conducted in cordial environment amongst the teachers taking the examination. Teachers taking such examinations should not have ill thoughts about each other and courtesies should be offered to each other in case of difference of opinion, which should be critically suppressed in front of the students.

5. Evaluation and marking system:

Basic honesty in the evaluation and marking system is absolutely essential and in the process impartial nature of the evaluator is required in the examination system to become. It is a primary responsibility of the teacher to see that right students who are really putting up lot of hard work with right kind of intelligence are correctly awarded.

The marking patterns should be justifiable to the students without any ambiguity and teacher should see that students are faced with just circumstances.